IN THE CLAIMS:

Claims 1-26 (Canceled)

27. (New) An apparatus, comprising:

an encoder configured to convert input data to a binary coded base system of an augmented code employing a base of an original code used for coding said input data, wherein said augmented code employs more symbols for coding than said original code, said encoder including:

an adder configured to add said input data to a multiplication product to generate a base sum that is binary-coded in said augmented code;

a multiplier configured to multiply an accumulated value by a base of said original code to provide said multiplication product that is binary-coded in said augmented code; and

an accumulator configured to employ said base sum to provide an accumulated value as an output for said encoder, wherein said accumulated value is binary-coded in said augmented code to represent said input data.

28. (New) The apparatus as recited in Claim 27 wherein said original code is a 4b5b code that uses 16 symbols denoted 0-F and said augmented code is a 4b5b code that uses 17 symbols denoted 0-F and S.

29. (New) The apparatus as recited in Claim 27 further comprising a converter configured to receive said input data as a packet stream and provide said input data to said adder.

30. (New) The apparatus as recited in Claim 27 wherein said converter is configured to simultaneously receive four bits of said input data.

31. (New) The apparatus as recited in Claim 27 wherein said converter receives said input data in descending order from a most significant bit to a least significant bit.

32. (New) The apparatus as recited in Claim 31 wherein said accumulator initializes said accumulated value to zero when receiving said most significant bit.

33. (New) The apparatus as recited in Claim 27 wherein said accumulator is configured to iteratively replace said accumulated value with said base sum until said base sum includes a least significant bit of said input data.

34. (New) The apparatus as recited in Claim 27 wherein said converter receives said input data as a block of 49 grouped bits to be encoded by said encoder.

35. (New) The apparatus as recited in Claim 34 wherein said encoder encodes said 49 grouped bits employing 12 symbols of said augmented code.

36. (New) The apparatus as recited in Claim 35 wherein 48 bits of said 49 grouped bits are packet bits.

37. (New) The apparatus as recited in Claim 35 wherein one bit of said 49 grouped bits is employed as a control message.

38. (New) An apparatus, comprising:

a transmitter configured to transmit a signal having a plurality of packets, said transmitter including:

a buffer configured to receive a stream of input data; and

an encoder configured to convert said input data to a binary coded base system of an augmented code employing a base of an original code used for coding said input data, wherein said augmented code employs more symbols for coding than said original code, said encoder including:

an adder configured to add said input data to a multiplication product to generate a base sum that is binary-coded in said augmented code;

a multiplier configured to multiply an accumulated value by a base of said original code to provide said multiplication product that is binary-coded in said augmented code; and

an accumulator configured to employ said base sum to provide an accumulated value as an output for said encoder, wherein said accumulated value is binary-coded in said augmented code to represent said input data.

39. (New) The apparatus as recited in Claim 38 wherein said original code is a 4b5b code that uses 16 symbols denoted 0-F and said augmented code is a 4b5b code that uses 17 symbols denoted 0-F and S.

40. (New) The apparatus as recited in Claim 38 wherein said encoder further comprises a converter configured to receive said input data as a packet stream from said buffer and provide said input data to said adder.

41. (New) The apparatus as recited in Claim 40 wherein said converter receives said input data in descending order from a most significant bit to a least significant bit.

42. (New) The apparatus as recited in Claim 41 wherein said accumulator initializes said accumulated value to zero when receiving said most significant bit.

43. (New) The apparatus as recited in Claim 38 wherein said accumulator is configured to iteratively replace said accumulated value with said base sum until said base sum includes a least significant bit of said input data.

44. (New) The apparatus as recited in Claim 38 wherein said converter receives said input data as a block of 49 grouped bits to be encoded by said encoder.

45. (New) The apparatus as recited in Claim 44 wherein said encoder encodes said 49 grouped bits employing 12 symbols of said augmented code.

46. (New) The apparatus as recited in Claim 45 wherein 48 bits of said 49 grouped bits are packet bits and one bit of said 49 grouped bits is employed as a control message.